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TOWNSEND and TOWNSEND and CREW LLP

By: [signature]

PATENT
Docket No.: 018865-001740US
Client Ref. No.: 17732.7226.001.001

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Confirmation No.: 9390
MO et al.	Examiner: HA, Nathan W.
Application No.: 10/630,249	Art Unit: 2814
Filed: July 30, 2003	COMMUNICATION PURSUANT TO EXAMINER INTERVIEW
For: FIELD EFFECT TRANSISTOR AND METHOD OF ITS MANUFACTURE	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

On October 23, 2007, the undersigned conducted a telephone interview with Examiner Nathan Ha. The following provides a summary of the substance of that interview.

The interview focused mainly on the various points of distinction between the claims and the prior art as presented in the response filed by the Applicants on November 20, 2006. In particular, the undersigned reiterated (1) the lack of any motivation to combine Chau with Hshieh '128 (the alleged motivation - "in order to facilitate hot electron injection" - being entirely unrelated to Chau's abrupt junction as well as any structure in Hshieh '128), and (2) that, even if combined, the combination would not result in the claimed structure, at least because Chau's abrupt junction is between the source and the body of a transistor which are regions having dopants of opposite conductivity type. Other grounds distinguishing the prior art from the claims as explained in the response filed on November 20, 2006 were also discussed briefly.

To further clarify some of the points of distinction, the undersigned submitted a proposed amendment by facsimile on June 14, 2007, as well as on October 18, 2007. The proposed amendment is submitted herewith as "Attachment #1." This proposed amendment, which was also discussed during the interview of October 23, 2007, adds language to independent claim 46 that expressly defines the abrupt junction as being formed "between the heavy body region having dopants of the second conductivity type and the dope well having dopants of the second conductivity type."

In response to the explanation by the undersigned that similar arguments regarding the term "abrupt junction" were successfully addressed during prosecution of the parent application, the Examiner requested a copy of the relevant papers from the parent prosecution history. Applicants submit herewith as "Attachment #2" a copy of a response dated June 7, 2001 (herein "6/7/01 Response") filed in parent application number 08/970,221, now U.S. patent number 6,429,481. The Examiner also indicated an interest in reviewing a declaration supporting commercial success as another objective measure of patentability, which was submitted with the 6/7/01 Response and is included in Attachment #2.

Applicants note that a different set of claims having different scope were the subject of the 6/7/01 Response and that a copy of the 6/7/01 Response is provided here solely for the purpose of further clarifying the distinction between an abrupt junction and a linearly graded junction, which is discussed in some detail in the 6/7/01 Response at pages 5-7. As was the case in the parent application 08/970,221, references to textbook analysis of different types of junctions are provided to assist the Examiner in better understanding the background of the technology and in particular the contrasts between the more common linearly graded junction and an abrupt junction. Therefore, the detailed analysis referenced from the textbook by Sze is not intended to be limiting of the scope of the claim language. As described in the instant application, an abrupt junction can be formed in different ways, and indeed the abrupt junction described by Sze is between regions having opposite polarity dopants, while the claimed abrupt junction is

formed between regions having the same polarity dopants. Accordingly, the sole purpose of submitting a copy of the 6/7/01 Response is to again highlight the fact that one of skill in this art understands that an abrupt junction has distinct structural and functional properties that differentiate it from the more common linearly graded junction.

Applicants thank the Examiner for the opportunity to discuss the application and invite the Examiner to call the undersigned if the Examiner believes a telephone conference would expedite prosecution of this application.

Respectfully submitted,

Babak S. Sani
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Attachments
BSS:deb
61196807 v1

ATTACHMENT #1

Application/Control Number 10/630,249

Proposed Amendment for Discussion with Examiner Nathan Ha, Art Unit 2814

June 14, 2007

46. (currently amended) A field effect transistor comprising:

a semiconductor substrate having dopants of a first conductivity type;

a trench extending a predetermined depth into the semiconductor substrate;

a doped well having dopants of a second conductivity type opposite to the first conductivity type and extending into the semiconductor substrate to form a well junction at a first depth;

a doped source region having dopants of the first conductivity type and extending into the semiconductor substrate to form a source junction at a second depth; and

a doped heavy body region having dopants of the second conductivity type and extending into the doped well to form a heavy body junction at a depth that is deeper than the source junction and shallower than the trench,

wherein the heavy body region forms an abrupt junction in the doped well, the abrupt junction being defined by the junction between the heavy body region having dopants of the second conductivity type and the doped well having dopants of the second conductivity type.

* * * COMMUNICATION RESULT REPORT (JUN. 13. 2007 8:26PM) * * *

FAX HEADER 1:
FAX HEADER 2:

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E-3) NO ANSWER
E-2) BUSY
E-4) NO FACSIMILE CONNECTION

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Date:	Client & Matter Number:	No. Pages (including this one): -2-
June 13, 2007	**018865-001740**	
To: **Examiner Nathan Ha Art Unit 2814**	At Fax Number: 571-273-1707	Confirmation Phone Number:

From: Babak S. Sani **(0225)**

Re: Application Number 10/630,249

Dear Examiner Ha,

The Applicant in the referenced application will be filing an RCE shortly. I would appreciate the opportunity to briefly discuss the attached amendment to the first independent claim (claim 46) tomorrow Thursday June 14, if possible. I will call you at 2:30 PM your time tomorrow in hopes that we can discuss this case.

Thank you.

Babak S. Sani

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61079975 v1

ATTACHMENT #2

PATENT
Attorney Docket No.: 18865-17US
Client Reference No.: 17732/722600

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Examiner: Jackson Jr., J.
Sze-Ki Mo, et al.	Art Unit: 2815
Application No.: 08/970,221	AMENDMENT
Filed: November 17, 1997	
For: FIELD EFFECT TRANSISTOR AND METHOD OF ITS MANUFACTURE	

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

In response to the Office Action mailed December 5, 2000, please amend the above-captioned patent application as set forth below.

IN THE CLAIMS:

Please cancel claims 13, 18-22 and 54 without prejudice to renewal and amend claims 1, 8, 47, 50, 53 and 55 as set forth below. A marked-up version of the amended claims is included at the end of the remarks section.

1. (Thrice Amended) A trenched field effect transistor comprising:

a semiconductor substrate having dopants of a first conductivity type;

a trench extending a predetermined depth into said semiconductor substrate;

a pair of doped source junctions having dopants of the first conductivity type, and positioned on opposite sides of the trench;

a doped well having dopants of a second conductivity type opposite to said first conductivity type, and formed into the substrate to a depth that is less than said predetermined depth of the trench; and

a doped heavy body having dopants of the second conductivity type, and positioned adjacent each source junction on the opposite side of the source junction from the trench, said heavy body extending into said doped well to a depth that is less than said depth of said doped well,

wherein the heavy body forms an abrupt junction with the well and the depth of the junction, relative to the depth of the well, is adjusted so that a transistor breakdown initiation point is spaced away from the trench in the semiconductor, when voltage is applied to the transistor.

8. (Thrice Amended) An array of transistor cells comprising:

a semiconductor substrate having a first conductivity type;

a plurality of gate-forming trenches arranged substantially parallel to each other, each trench extending a predetermined depth into said substrate and the space between adjacent trenches defining a contact area;

a pair of doped source junctions, positioned on opposite sides of the trench and extending along the length of the trench, the source junctions having the first conductivity type;

a doped well having a second conductivity type with a charge opposite that of the first conductivity type, the doped well formed in the semiconductor substrate between each pair of gate-forming trenches;

a doped heavy body having the second conductivity type formed inside the doped well and positioned adjacent each source junction, the deepest portion of said heavy body extending less deeply into said semiconductor substrate than said predetermined depth of said trenches; and

alternating heavy body and source contact regions defined at the surface of the semiconductor substrate along the length of the contact area,

wherein the heavy body forms an abrupt junction with the well, and a depth of the heavy body relative to a depth of the well is adjusted so that breakdown of the transistor originates in the semiconductor in a region spaced away from the trenches when voltage is applied to the transistor.

47. (Twice Amended) A trenched field effect transistor formed on a substrate, comprising:

a plurality of trenches formed in parallel along a longitudinal axis, the plurality of trenches extending into the substrate to a first depth;

a doped well extending into the substrate between each pair of trenches;

a pair of doped source regions formed on opposite sides of each trench; and

a doped heavy body formed inside the doped well adjacent each source region, the doped heavy body extending into the doped well to a second depth that is less than the first depth,

wherein the doped heavy body:

forms a continuous doped region along substantially the entire longitudinal axis of a trench, and

forms an abrupt junction with the well, and a depth of the heavy body junction relative to a maximum depth of the well, is adjusted so that a peak electric field in the substrate is spaced away from the trench when voltage is applied to the transistor.

50. (Twice Amended) The trenched field effect transistor of claim 1 further comprising an epitaxial layer having dopants of the first conductivity type, and formed between the substrate and the doped well, with no buried layer formed at an interface between the epitaxial layer and the substrate.

53. (Once Amended) The trenched field effect transistor of claim 8, further comprising:

an epitaxial layer having the first conductivity type formed between the substrate and the well, with no buried layer formed at an interface between the epitaxial layer and the substrate.

55. (Once Amended) The trenched field effect transistor of claim 47, further comprising:

an epitaxial layer having the first conductivity type formed between the substrate and the well,

wherein the second depth relative to a depth of the well is adjusted to eliminate the need for any layers disposed between the epitaxial layer and the substrate.

REMARKS

Upon entry of this amendment, which cancels claim 13, 18-22 and 54 without prejudice to renewal and amends claims 1, 8, 47, 50, 53 and 55, claims 1, 2, 5-12, 14-17, 46-53 and 55 remain pending. Previously examined claims 50, and 53-55 were rejected under 35 U.S.C. 112, second paragraph, for being indefinite, claims 1, 2, 6, 8-11, 46-53, 55 were rejected under 35 U.S.C. 103(a) as being anticipated by or in the alternative obvious over USPN 5,629,543 to Hshieh et al. (hereinafter Hshieh '543); claim 7 was rejected as being unpatentable over Hsheih '543 in view of USPN 5,688,725 to Darwish et al. (Darwish '725); and claims 1, 2, 5-12, 14-22, 46-55 were rejected as being unpatentable over Hshieh '543 with Darwish '725, applicant's prior art admissions, Nakamura '491, Bencuya '324 and Harada '050. Reconsideration of the claims in view of the above amendments and the comments below is respectfully requested.

The Rejections

- Section 112, 2nd ¶

Claims 50 and 53-55 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite. The rejection states that "the recitation 'wherein the relative depths ... are controlled to eliminate the need for any layers ...' are vague and indefinite of exact structure." The rejection asks "what is the exact structure determined by 'controlled...'?"

These claims were added for the specific purpose of further distinguishing over the cited reference Hshieh '543. Hshieh '543 teaches forming an N+ buried layer (16) between the epitaxial N- layer (or drift region 4B) and the substrate 10 to ensure "that avalanche breakdown occurs at the buried layer/body region ...." [Hshieh '543, col. 2, lines 6-10]. Applicants were the first to find that a trench transistor structure can be formed with a shallow heavy body structured in a way that the need for such buried layers is eliminated with very little, if any, compromise in the transistor cell density. Applicants respectfully submit that, for the reasons discussed below, there should be no ambiguity associated with the claimed structure which specifies the relative depths of the heavy body and the well regions in the trench transistor (see below). Applicants have nevertheless amended claims 50, 53 and 55 to remove the language the rejection finds vague. Withdrawal of this rejection is therefore respectfully requested.

- Section 102(e) or 103(a): Hshieh '543

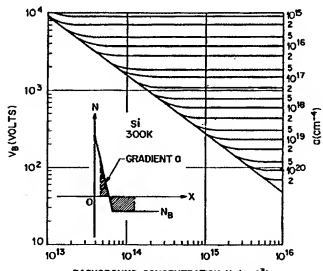
The Office Action maintains the previous rejection of claims 1, 2, 6, 8-11, 46-53, and 55 under 35 U.S.C. §102(e) as anticipated by or, in the alternative, under 35 U.S.C. §103(a) as obvious over Hshieh '543. The rejection states:

> "Applicant's argument that Hshieh does not disclose an 'abrupt' junction is unpersuasive. The junction in Hshieh is abrupt. There are no particularly claimed dopant concentrations which would structurally distinguish applicant's 'abrupt' junctions over the 'abrupt' junctions of the applied art. Accordingly 'abrupt' is merely a label which does not structurally distinguish applicant's claims over the applied art."

Applicants respectfully submit that this rejection not only mischaracterizes the technical import of the claim language, it misconstrues well-established law regarding adequacy of claims. The terminology "abrupt junction" is well-known to those skilled in the art as having a very well-defined meaning with specific structural significance. "Physics of Semiconductor Devices," by S.M.Sze is considered a seminal book on the subject and is widely used throughout the academic community as well as the industry. Sze devotes an entire section (section 2.3.1) on the "Abrupt Junction," and states the following at page 72: "In

practice, most impurity profiles can be approximated by the following two limiting cases: the abrupt junction and the linearly graded junction ...." Sze also explains the "profound effects" of these differently formed junctions on the "avalanche multiplication process." [Sze, bottom of page 73]. After a detailed analysis of the characteristics of the "abrupt" junction versus the "linearly graded" junction, at page 104, Sze presents the following:

> "An approximate universal expression can be given as follows for the results above comprising all semiconductors studied: :
>
> $$V_B \cong 60(E_g/1.1)^{3/2}(N_B/10^{16})^{-3/4} \quad V \qquad (79a)$$
>
> for abrupt junctions where E_g is the room-temperature bandgap in eV, and N_B is the background doping in cm-3; and
>
> $$V_B \cong 60(E_g/1.1)^{6/5}(a/3x10^{20})^{-2/5} \quad V \qquad (79b)$$
>
> for linearly graded junctions where a is the impurity gradient in cm-4.
>
> For diffused junctions with a linear gradient on one side of the junction and a constant doping on the other side (shown in Fig. 31, insert), the breakdown voltage lies between the two limiting cases considered previously 39 (Figs. 26 and 28). For large a and low N_B, the breakdown voltage of diffused junctions (Fig. 31) is given by the abrupt junction results (bottom line); on the other hand, for small a and high N_B, V_B will be given by the linearly graded junction results (parallel lines)."



Accordingly, referring to Fig. 31 of Sze (reproduced above for convenient reference), for a given background doping N_B, the breakdown voltage V_B is lowered (parallel lines) as the impurity gradient *a* increases until it comes to a limit at the point (on the bottom line) where the impurity gradient *a* reaches an abrupt junction, after which V_B remains constant. Thus, contrary to the rejection's characterization, "abrupt" is clearly neither "merely a label" nor is it devoid of any structural significance.

Furthermore, the rejection's assertion that "there are no particularly claimed dopant concentrations which would structurally distinguish applicant's 'abrupt' junctions over the 'abrupt' junctions of the prior art" is flawed in two respects. First, no where in Hshieh '543 could there be found any mention of any junction being "abrupt." Secondly, it is well-established that mathematical precision should not be imposed on claim language for its own sake, and that an applicant has the right to claim the invention in terms that would be understood by persons of skill in the field of invention. *Modine Mfg. Co. v. United States ITC*, 75 F.3d 1545, 37 USPQ2d 1609 (Fed. Cir. 1996). This is particularly relevant in the present case where not only the structural significance of the terminology "abrupt junction" is well understood by those skilled in this art, the number of different variables involved in a structure that is an "abrupt junction" (e.g., background doping, gradient, target breakdown voltage, etc.) renders it meaningless to provide, for example, specific doping concentrations without specifying numbers for other variables. Furthermore, any numbers would also be rendered meaningless given the well-known and ever aggressive miniaturization process over time in the field of semiconductors. Dimensions such as junction depths employed in semiconductor devices at any given time often become obsolete within a two to three year period. In fact, products that are now being manufactured based on the teachings of the instant invention no longer employ the exemplary numbers provided in the instant specification (filed in November of 1997). Thus, requiring specific doping concentrations or other mathematical limitations where none should be required would unnecessarily and unfairly limit the scope of the claim applicants are otherwise entitled to.

Independent claims 1, 8 and 47 all specify the junction formed between the "heavy body" and the "well" as being "abrupt" and, for the above reasons, therefore distinguish over the cited art. These claims, however, include additional elements that further distinguish over the cited references. Claim 1, for example, also recites "the depth of the [heavy body] junction relative to the depth of the well, is adjusted so that a transistor breakdown initiation point is spaced away from the trench ...." Again, no combination of the cited prior art teaches or suggests the claimed structure. In maintaining its rejection of the claim, however, the Office Action states: " Arguments regarding 'controlled' are unconvincing of patentability because the claimed structure does not functionally or structurally distinguish over the applied art." It is difficult to follow the reasoning behind this rejection since the relevant claim language, on its face, does clearly distinguish in both those respects. Structurally, the relevant claim language defines a specific depth for the "heavy body," and functionally, it specifies the moving away or spacing away of the "transistor breakdown initiation point ... from the trench." Contrary to the rejection's assertion, this combination clearly distinguishes over the cited references. With respect to the depth of the P+ region 24 in Hshieh '543, a reading of Hshieh '543 makes it clear that the inventors had no clue whatsoever about the possibility of having a P+ region (24) that is shallower than the well (18) and yet is capable of addressing the breakdown problem by its structure (i.e., depth and abruptness of its junction). This is so because Hshieh '543 clearly shows a P+ region 24 that is as deep or deeper than the well 18 in every figure, and in the only instance where they make a cursory mention of shallower "P+ body contact regions 24", they immediately add "... in which case the breakdown current conduction path is from body region 18 to buried layer 16." [Hshieh '543, col. 3, lines 1-6]. Hshieh '543 therefore teaches nothing more than what was already known in the art; that if the P+ body region 24 is made shallower than the well, the device would then need some other additional structure to control the point of breakdown initiation (see further discussion below). This additional structure, as taught by Hshieh '543, is an N+ buried layer 16. Hshieh '543 therefore clearly fails to teach or suggest a heavy body that is shallower than the well, and has its depth "relative to the depth of the well, [] adjusted so that a transistor breakdown initiation point is spaced away from the trench ...."

Although not clear, in light of the §112, 2nd ¶ rejection above, it is assumed that the Examiner may have had difficulty with the use of the word "controlled." While it is not deemed necessary, to the extent that the Examiner may consider "adjusted" more appropriate in defining a structure, Applicants have amended independent claims 1, 8 and 47 to replace the word "controlled" with "adjusted." Applicants are entitled to claim this structural aspect of the present invention (i.e., relative depths of the heavy body and the well), that is also further defined functionally (impacting breakdown initiation point), without having to limit the claim to specific numerical dimensions. Applicants welcome Examiner's suggestions for any substitute words for "controlled" or "adjusted."

Hshieh '543 thus clearly neither teaches a trench field effect transistor with a "heavy body" that forms an "abrupt junction" with the well, nor one that has a "heavy body" with a depth relative to the depth of the well that causes "a transistor breakdown initiation point [to move] away from the trench." Nor does Hshieh '543 even remotely suggest the claimed combination. In fact, by teaching that a buried layer (16) is required to address the breakdown problem, Hshieh '543 teaches away from a structure that can accomplish similar functionality with a clever expedient as that of the claimed "heavy body." To be sure, the notion that a prior art diagram may "look similar" to a diagram that depicts an aspect of the invention, cannot be the basis for a 102 or 103 rejection. Often times diagrams are not to scale and significant novel and non-obvious structural features such as depth or abruptness of a junction in semiconductor technology may not be easily depicted. Again, both the diagrams and the body of Hshieh '543 not only fail to teach but also fail to suggest the claimed invention.

Independent claims 1, 8 and 47 are thus patentably distinguished over Hshieh '543. Claims 2, 5-7, 9-12, 14-17, 46, 48-53 and 55 depend from one the claims 1, 8 and 47 and therefore derive patentability therefrom. These claims, however, recite additional novel and non-obvious features that further distinguish over Hshieh '543. Claims 48 and 49, for example, describe an alternating source and heavy body contact arrangement along the longitudinal axis of a trench. No such structure is taught or suggested by Hshieh '543. Claims

50, 53 and 54, for example, specifically recite a heavy body which has its depth relative to the depth of the well "adjusted to eliminate the need for any layers disposed between the epitaxial layer and the substrate." Hshieh '543 teaches the opposite: forming a "buried layer" (16) between the epitaxial layer (or drift region) and the substrate. Claims 1-2, 5-12, 14-17, 46-53 and 55 are therefore patentably distinguished over Hshieh '543. Accordingly, withdrawal of this rejection is respectfully requested.

- Section 103(a): Hshieh '543, Darwish '725, Nakamura '491, Bencuya '324, and Harada '050

Claims 1, 2, 5-12, 14-22, 46-55 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Hshieh '543 with Darwish '725, applicant's prior art admissions, Nakamura '491, Bencuya '324, and Harada '050. The rejection does not provide an explanation of any new grounds of rejection other than to state: "Harada additionally teaches a termination structure including a deep well connected to body regions. It would have been obvious to have practiced the same with Hshieh to have improved breakdown voltage. The previous rejection with the above comments applies."

With respect to claims 1, 8 and 47, and all claims depending therefrom, as discussed above, Hshieh '543 clearly fails to teach or suggest the invention as claimed. None of the other cited references, or any combination thereof, including any admitted prior art, adds anything that would support a finding of unpatentability. If anything, a close look at every one of these references, as well as many of the other relevant prior art of record, provides overwhelming evidence of non-obviousness of the claimed invention. This is so because these prior art references, one after another, demonstrate the fact that many of the most skilled artisans in the field recognized and struggled with the exact same set of challenges (e.g., increased trench MOSFET cell density, improved breakdown voltage, lowered transistor on-resistance, etc.), yet none were able to conceive of the solution claimed by the present invention. Instead, in each instance, the prior art proposes a solution that is fundamentally different both structurally and functionally, as well as being technically inferior as demonstrated by the commercial success of the products manufactured based on the present invention. To stress this point, Applicants present below a brief analysis of a number of the

cited prior art references. A declaration evidencing the commercial success as another objective measure of non-obviousness is separately submitted.

- **Hshieh '543**

An analysis of this reference has already been presented, however, since it forms the main basis for rejection of the claims, it is repeated here in a more concise fashion.

Recognition of the Problem:

"However it is also known that when cell density is high as in the typical trenched transistor structure, a new undesirable JFET phenomenon gradually appears between the P+ deep body regions 5. The P+ deep body regions 5 typically extend from a principal surface of the semiconductor material into the P body region 7 to provide a contact to the P body region 7. These deep body regions 5 ensure that avalanche breakdown occurs in these regions rather than at the bottom of the trenches. This undesirable JFET phenomenon is because such deep body regions 5 are relatively close to each other. (Also shown in FIG. 1 are conventional drain electrode 8B and source-body electrode 8A.) Thus while avalanche breakdown occurs rather than destructive breakdown at the trench bottom, i.e. breakdown damaging the insulating oxide at the trench bottom, undesirably this new JFET resistance makes a bigger contribution to drain-source on resistance when cell density is higher." [Col. 1, lines 29-49, emphasis added].

Proposed Solution (Figs. 2 & 3F):

"Further, in accordance with the invention a doped buried layer [16]is formed in the upper portion of the drain region [10] and in contact with the drift region [14]. This buried layer has the same doping type as that of the drain region and a doping concentration higher than that of the drift region, and is typically located to directly underlie the body contact (deep body) region formed between each pair of adjacent source regions. The buried layer is heavily doped to form N+ doped fingers extending into the drift region. This buried layer [16] is typically formed prior to the epitaxial growth of the drift region, and by having an optimized doping profile ensures that avalanche breakdown occurs at the buried layer/body region or buried layer/body contact region. Hence the distance between the lower part of the body contact or body region and the upper part of the buried layer determines breakdown." [Col. 1, line 65 to col. 2, line 13, reference numerals and underlining added].

- Darwish '725

Recognition of the Problem:

"The deep central P+ region 114 in MOSFET 300, while greatly reducing the adverse consequences of breakdown, also has some unfavorable effects. First, an upward limit on cell density is created, because with increasing cell density P ions may be introduced into the channel region. As described above, this tends to increase the threshold voltage of the MOSFET. Second, the presence of a deep P+ region 114 tends to pinch the electron current as it leaves the channel and enters the drift region 111. In an embodiment which does not include a deep P+ region (as shown in, for example, FIG. 2A), the electron current spreads out when it reaches the drift region 111. This current spreading reduces the average current per unit area in the drift region 111 and therefore reduces the on-resistance of the MOSFET. The presence of a deep central P+ region limits this current spreading and increases the on-resistance consistent with high cell densities. What is needed, therefore, is a MOSFET which combines the breakdown advantages of a deep central P+ region with a low on-resistance." [Col. 3, lines 28-48, emphasis added].

Proposed Solution (Figs 4 & 5):

"When the MOSFET is turned on, an electron current flows vertically through a channel within the body region adjacent the trench. To promote current spreading at the lower (drain) end of the channel region when the MOSFET is turned on, a "delta layer" [402] is provided within the drift region. The delta layer is a layer wherein the concentration of dopant of first conductivity type is greater than the concentration of dopant of first conductivity type in the drift region generally. In many embodiments the delta layer abuts the body region, although in some embodiments the delta layer is separated from the body region. The upper boundary of the delta layer is at a level which is above the bottom of the trench in which the gate is formed. In some embodiments, the upper boundary of the delta layer coincides with a lower junction of the body region. The lower boundary of the delta layer may be at a level either above or below the bottom of the trench." [Col. 3, lines 64 to col. 4, line 13, reference numeral and underlining added].

- Hshieh '128 (Office Action mailed 8/4/99)

Recognition of the Problem:

"In typical DMOS transistors using a trenched gate electrode, in order to avoid destructive breakdown occurring at the bottom of the trench into

the underlying drain region, such transistors are fabricated so that a P+ deep body region extends deeper than does the bottom of the trench into the substrate (drain region). Thus rather than destructive breakdown occurring at the trench bottom, instead avalanche breakdown occurs from the lowest portion of this P+ deep body region into the underlying drain region. However due to device physics limitations, the cell density of such transistors is thereby restricted by lateral diffusion of this P+ deep body region. That is, in order to provide a P+ deep body region that extends deep enough into the substrate, the drive in step causes this P+ deep body region to diffuse laterally. If it diffuses too far laterally, it may coalesce with an adjacent P+deep body region and degrade transistor performance.

Hence, in order to allow deep enough extension of the P+deep body region into the substrate, the transistor cells each must be relatively large in surface area so that the lateral diffusion does not allow such coalescing. This increases the surface area consumed by each cell, or in other words increases the size of the transistor. As is well known, it is a primary goal of power MOSFET fabrication to minimize chip surface area. This lateral diffusion of the P+deep body region prevents optimization of transistor density and hence wastes chip surface area." [Col. 1, lines 25-51, emphasis added].

Proposed Solution (Figs. 1, 2 & 3):

In accordance with the invention, cell density is increased in a DMOS transistor. In some embodiments this is accomplished by providing a very narrow (in lateral dimension) P+deep body region [16 in Fig. 1] with little or no lateral diffusion. ... In a second embodiment, in addition to the high energy P+deep body implant [36 in Fig. 2], a double epitaxial layer [12 and 34 in Fig. 2]is provided underlying the body region [14], with the P+deep body P+region [34] not extending below the depth of the trench. Instead, the double epitaxial layer provides the desired current path away from the bottom of the trenches. ... In a third embodiment, there is no P+deep body implantation at all and instead only the double epitaxial layer [12 & 34 in Fig. 3] is used underneath the body region." [Col. 1, lines 54 to col. 2, line 19, reference numerals and underlining added].

Two more examples of prior art references evidencing the fact that designers attempting to solve the same problem have failed to arrive at a solution that is even remotely suggestive of the present invention are provided below. An earlier issued patent (USPN 5,072,266) illustrates the fact that the specific challenges have been known for well over a

decade, and a second more recently issued patent (USPN 5,998,836) shows a contemporaneous attempt at solving the problem. Both offer solutions that are widely different than that proposed and claimed by the present invention.

- **5,072,266 (Bulucea et al.)**

Recognition of the Problem:

"An engineering trade-off must be made between on-resistance, breakdown voltage and other engineering figures of merit so that the perimeter-to-area ratio Z/A advantage of the open-cell is lost. Given these constraints, the closed-cell geometry appears to be more practical. However, the closed cell geometry has at least three associated problems that do no appear to have been reported on in the technical or patent literature. The first problem is semiconductor surface breakdown. ... This junction is thus exposed to electric field line crowding and to breakdown in the epitaxial material adjacent to the bottom corners of the trench, when the device is biased in the BVDSS condition." [Col. 4, lines 24-41, emphasis added].

Proposed Solution (Fig. 8):

"This invention provides an optimized version of a power metal-oxide-semiconductor field-effect transistor (MOSFET) [wherein bulk] breakdown voltage is achieved by using a two-dimensional, field shaping, dopant profile that includes a central deep p+ (or n+) layer [27c] that is laterally adjacent to a p body layer ...." [Col. 1, lines 50-61, reference numeral and emphasis added].

"FIG. 8 illustrates one embodiment of the invention, showing half of a hexagonally shaped trench DMOS structure 21. The structure includes ... a body region 27 [where] a central portion 27c of the body region lies below a plane that is defined by the bottom of the trench 29 for the transistor cell." [Col. 6, lines 28-60]

- **5,998,836 (Williams)**

Recognition of the Problem:

"Two critical characteristics of a power MOSFET are its breakdown voltage, i.e., the voltage at which it begins to conduct current when in an off condition, and its on-resistance i.e., its resistance to current flow

when in an on condition. The on-resistance of a MOSFET generally varies directly with its cell density, since when there are more cells per unit area there is also a greater total "gate width" (around the perimeter of each cell) for the current to pass through. The breakdown voltage of a MOSFET depends primarily on the doping concentrations and locations of the source, body and drain regions in each MOSFET cell." [Col. 1, lines 32-44, emphasis added].

Proposed Solution (Fig. 3):

"In accordance with this invention, there is created in the chip a protective diffusion of the second conductivity type [38], which forms a PN junction [39] with first conductivity material in the epitaxial layer [14] or substrate. This PN junction functions as a diode. A metal layer [36] ties the protective diffusion (i.e., one terminal of the diode) to the source regions [34] of the MOSFET cells such that the diode is connected in parallel with the channels of the MOSFET cells." [Col. 2, lines 60 to 68, reference numerals and underlining added].

The above analysis holds true for many of the other prior art references of record. This demonstrates that for well over a decade engineers in the field have attempted to arrive at a design for a trench MOSFET that addresses breakdown voltage, on-resistance and cell density in an optimized fashion. It also demonstrates that time and again a solution is proposed that is very different than that found by the Applicants. If the present invention as claimed were obvious, as the rejection contends, one would have to ask why then did no person of skill in the art arrive at this solution years ago. One answer to this question may be the fact that there has been a general understanding by those skilled in this art that, in terms of impact on the electric field, between the deeper well (or body) region and a heavily doped body region that is shallower than the well, the deeper well region (that is closest to the epitaxial layer) dominates. This had led to a generally accepted assumption that such shallow heavy body junction inside a graded body junction, no matter how deep, could not have any measurable impact on breakdown voltage.

Challenging these and other accepted assumptions, and through exhaustive experimentation and computer simulations, Applicants were the first to find that the problem can in fact be addressed optimally by employing, in combination with the other features of the

transistor, a shallow heavy body with specific depth and junction characteristics. The solution offered by the instant invention requires no additional structures as proposed by numerous prior art references such as buried layers or dual epitaxial layers, delta layers, protective PN junction diodes, deep P+ body regions, etc. A family of trench MOSFET products embodying the Applicants' elegant solution, which has clearly not been taught or suggested by the art of record, has enjoyed tremendous commercial success as a direct result of the benefits of the claimed invention. To provide further objective evidence of non-obviousness of the claimed invention, Applicants herewith submit a declaration by the Senior Vice President of Discrete Power Products of the Assignee demonstrating this commercial success.

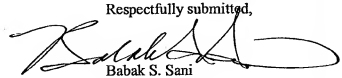
Accordingly, none of the cited references, or any combination thereof, teach or suggest a trench transistor having a "heavy body" that forms an "abrupt junction" inside a well, and whose depth is adjusted to impact the location of breakdown initiation. Every independent claim pending in the instant application recites this combination. All pending claims are therefore patentably distinguished over the art or record. Withdrawal of this rejection is respectfully requested.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,



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Marked-Up Version of Amended Claims – Appln. No. 08/970,221

2. (Thrice Amended) A trenched field effect transistor comprising:

a semiconductor substrate having dopants of a first conductivity type;

a trench extending a predetermined depth into said semiconductor substrate;

a pair of doped source junctions having dopants of the first conductivity type, and positioned on opposite sides of the trench;

a doped well having dopants of a second conductivity type opposite to said first conductivity type, and formed into the substrate to a depth that is less than said predetermined depth of the trench; and

a doped heavy body having dopants of the second conductivity type, and positioned adjacent each source junction on the opposite side of the source junction from the trench, said heavy body extending into said doped well to a depth that is less than said depth of said doped well,

wherein the heavy body forms an abrupt junction with the well and the depth of the junction, relative to the depth of the well, is **[controlled]** adjusted so that a transistor breakdown initiation point is spaced away from the trench in the semiconductor, when voltage is applied to the transistor.

8. (Thrice Amended) An array of transistor cells comprising:

a semiconductor substrate having a first conductivity type;

a plurality of gate-forming trenches arranged substantially parallel to each other, each trench extending a predetermined depth into said substrate and the space between adjacent trenches defining a contact area;

a pair of doped source junctions, positioned on opposite sides of the trench and extending along the length of the trench, the source junctions having the first conductivity type;

a doped well having a second conductivity type with a charge opposite that of the first conductivity type, the doped well formed in the semiconductor substrate between each pair of gate-forming trenches;

a doped heavy body having the second conductivity type formed inside the doped well and positioned adjacent each source junction, the deepest portion of said heavy body extending less deeply into said semiconductor substrate than said predetermined depth of said trenches; and

alternating heavy body and source contact regions defined at the surface of the semiconductor substrate along the length of the contact area,

wherein the heavy body forms an abrupt junction with the well **[junction]**, and a depth of the heavy body relative to a depth of the well**[,] is [controlled]** adjusted so that breakdown of the transistor originates in the semiconductor in a region spaced away from the trenches when voltage is applied to the transistor.

47. (Twice Amended) A trenched field effect transistor formed on a substrate, comprising:

a plurality of trenches formed in parallel along a longitudinal axis, the plurality of trenches extending into the substrate to a first depth;

a doped well extending into the substrate between each pair of trenches;

a pair of doped source regions formed on opposite sides of each trench; and

a doped heavy body formed inside the doped well adjacent each source region, the doped heavy body extending into the doped well to a second depth that is less than the first depth,

wherein the doped heavy body:

forms a continuous doped region along substantially the entire longitudinal axis of a trench, and

forms an abrupt junction with the well, and a depth of the heavy body junction**[,]** relative to a maximum depth of the well, **is [controlled]** adjusted so that a peak electric field in the substrate is spaced away from the trench when voltage is applied to the transistor.

50. (Twice Amended) The trenched field effect transistor of claim 1 further comprising an epitaxial layer having dopants of the first conductivity type, and formed between the substrate and the doped well, with no buried layer formed at an interface between the epitaxial layer and the substrate

[wherein the the relative depths of the doped heavy body and the well are controlled to eliminate the need for any layers disposed between the epitaxial layer and the substrate].

53. (Once Amended) The trenched field effect transistor of claim 8, further comprising:

an epitaxial layer having the first conductivity type formed between the substrate and the well, with no buried layer formed at an interface between the epitaxial layer and the substrate

[wherein the relative depths of the deepest portion of the heavy body and a depth of the well are controlled to eliminate the need for any layers disposed between the epitaxial layer and the substrate].

55. (Once Amended) The trenched field effect transistor of claim 47, further comprising:

an epitaxial layer having the first conductivity type formed between the substrate and the well,

wherein the second depth relative to **[and]** a depth of the well **[are controlled]** is adjusted to eliminate the need for any layers disposed between the epitaxial layer and the substrate.

PATENT
Attorney Docket No.: 18865-17US
Client Reference No.: 17732/722600

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Examiner: Jackson Jr., J.
Sze-Ki Mo, et al.	Art Unit: 2815
Application No.: 08/970,221	
Filed: November 17, 1997	
For: FIELD EFFECT TRANSISTOR AND METHOD OF ITS MANUFACTURE	DECLARATION OF IZAK BENCUYA

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

I, Izak Bencuya, declare as follows:

I have read and understood the present application, including the claims in their current state. The claims are attached to this Declaration as Attachment 1.

I am employed by Fairchild Semiconductor Corporation ("Fairchild"), and hold the position of Senior Vice President of Discrete Power Products. I have held that position since January, 2000.

Fairchild manufactures a family of trench power transistor ("trench MOSFET") products including FDS 6680A, FDS 6612A and FDS 6690A. These trench MOSFET products embody the trench transistor technology as set forth in the attached claims.

Part of my responsibility as the Vice President of Discrete Power is to oversee the development, sales and marketing of these products, as well as to acquire feedback from customers using the same. To this end, I have closely monitored the volume of sales as well as adoption rate and competitor response in order to determine the market acceptance and customer reaction to these products.

By the end of 1997 trench MOSFET technology was approximately 7-8% of the overall power MOSFET market. Siliconix Incorporated ("Siliconix"), as one of the largest manufacturers of power MOSFET devices, owned approximately 85% of the trench MOSFET market. Siliconix is also the assignee of several of the patents cited throughout the prosecution of the instant application including Hshieh '543, Hshieh '128 and Darwish '725.

Fairchild introduced its first trench power MOSFET product FDS6680 in January 1998. The design of FDS6680 is based on the features that are the subject of the claims in the instant application. In little over three years since the introduction of the Fairchild FDS6680, trench MOSFET technology has grown to 15% of the overall power MOSFET market, and Siliconix's share of that market is now about 50% with Fairchild owning 30% of the market.

This dramatic growth in the trench power MOSFET market and the success of the family of Fairchild trench MOSFET products can be directly attributed to the manufacturing and performance advantages of the Fairchild trench MOSFET technology made possible primarily by those technical aspects of the technology that are the subject of the attached claims.

The superior performance of the Fairchild trench products and the subsequent industry approval is further evidenced by favorable product reviews published in a number of major trade press publications. The following lists but a few examples of such publications, copies of which are attached herewith:

"Power FETs in Pentium push," Steve Bush, Electronics Weekly, UK, February 25, 1998

"Fairchild Offers 9mΩ Power MOSFET," Kenji Tsuda, Nikkei Electronics Asia, May 1998

"Flexible resistance in trench technology," Nick Flaherty, Electronics Times, UK, February 23, 1998

"PowerTrench mosfets deliver lowest on-resistance plus fast switching," Components in Electronics," April 1998

Elecronic Engineering Times / Taiwan, March 2, 1998

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date: 5/31/01

Izak Bencuya

SF 1230264 v1

ATTACHMENT 1

Claims as Pending – Appln. No. 08/970,221 – filed 11/17/97

1. A trenched field effect transistor comprising:

a semiconductor substrate having dopants of a first conductivity type;

a trench extending a predetermined depth into said semiconductor substrate;

a pair of doped source junctions having dopants of the first conductivity type, and positioned on opposite sides of the trench;

a doped well having dopants of a second conductivity type opposite to said first conductivity type, and formed into the substrate to a depth that is less than said predetermined depth of the trench; and

a doped heavy body having dopants of the second conductivity type, and positioned adjacent each source junction on the opposite side of the source junction from the trench, said heavy body extending into said doped well to a depth that is less than said depth of said doped well,

wherein the heavy body forms an abrupt junction with the well and the depth of the junction, relative to the depth of the well, is adjusted so that a transistor breakdown initiation point is spaced away from the trench in the semiconductor, when voltage is applied to the transistor.

2. The trenched field effect transistor of claim 1 wherein said doped well has a substantially flat bottom.

5. The trenched field effect transistor of claim 1 wherein said trench has rounded top and bottom corners.

6. The trenched field effect transistor of claim 1 wherein the abrupt junction causes the transistor breakdown initiation point to occur in the area of the junction, when voltage is applied to the transistor.

7. The trenched field effect transistor of claim 6 wherein said doped heavy body has a first dopant concentration near the abrupt junction and a second dopant concentration near its upper surface that is less than the first dopant concentration.

8. An array of transistor cells comprising:

a semiconductor substrate having a first conductivity type;

a plurality of gate-forming trenches arranged substantially parallel to each other, each trench extending a predetermined depth into said substrate and the space between adjacent trenches defining a contact area;

a pair of doped source junctions, positioned on opposite sides of the trench and extending along the length of the trench, the source junctions having the first conductivity type;

a doped well having a second conductivity type with a charge opposite that of the first conductivity type, the doped well formed in the semiconductor substrate between each pair of gate-forming trenches;

a doped heavy body having the second conductivity type formed inside the doped well and positioned adjacent each source junction, the deepest portion of said heavy body extending less deeply into said semiconductor substrate than said predetermined depth of said trenches; and

alternating heavy body and source contact regions defined at the surface of the semiconductor substrate along the length of the contact area,

wherein the heavy body forms an abrupt junction with the well, and a depth of the heavy body relative to a depth of the well is adjusted so that breakdown of the transistor originates in the semiconductor in a region spaced away from the trenches when voltage is applied to the transistor.

9. The array of transistor cells of claim 8, wherein each said doped well has a substantially flat bottom.

10. The array of transistor cells of claim 8 wherein the controlled depth of the junction causes the breakdown origination point to occur approximately halfway between adjacent gate-forming trenches.

11. The array of transistor cells of claim 8 wherein each said doped well has a depth less than the predetermined depth of said gate-forming trenches.

12. The array of transistor cells of claim 8 wherein each said gate-forming trench has rounded top and bottom corners.

14. The array of transistor cells of claim 8 further comprising a field termination structure surrounding the periphery of the array.

15. The array of transistor cells of claim 14 wherein said field termination structure comprises a well having a depth greater than that of the gate-forming trenches.

16. The array of transistor cells of claim 14 wherein said field termination structure comprises a termination trench extending continuously around the periphery of the array.

17. The array of transistor cells of claim 16 wherein said field termination structure comprises a plurality of concentrically arranged termination trenches.

46. The array of transistor cells of claim 8 wherein the doped heavy body forms a continuous doped region along substantially the entire length of said contact area.

47. A trenched field effect transistor formed on a substrate, comprising:

a plurality of trenches formed in parallel along a longitudinal axis, the plurality of trenches extending into the substrate to a first depth;

a doped well extending into the substrate between each pair of trenches;

a pair of doped source regions formed on opposite sides of each trench; and

a doped heavy body formed inside the doped well adjacent each source region, the doped heavy body extending into the doped well to a second depth that is less than the first depth,

wherein the doped heavy body:

forms a continuous doped region along substantially the entire longitudinal axis of a trench, and

forms an abrupt junction with the well, and a depth of the heavy body junction relative to a maximum depth of the well, is adjusted so that a peak electric field in the substrate is spaced away from the trench when voltage is applied to the transistor.

48. The trenched field effect transistor of claim 47 further comprising source and heavy body contact areas defined on a surface of the substrate between each pair of trenches.

49. The trenched field effect transistor of claim 48 wherein the contact areas alternate between source and heavy body contacts.

50. The trenched field effect transistor of claim 1 further comprising an epitaxial layer having dopants of the first conductivity type, and formed between the substrate and the doped well, with no buried layer formed at an interface between the epitaxial layer and the substrate.

51. The trenched field effect transistor of claim 1 wherein said doped heavy body is formed by a double implant of said dopant of the second conductivity type.

52. The trenched field effect transistor of claim 51 wherein said double implant comprises a first high energy implant to reach said second depth, and a second lower energy implant to extend the heavy body from said second depth to substantially a surface of the substrate.

53. The trenched field effect transistor of claim 8, further comprising:

an epitaxial layer having the first conductivity type formed between the substrate and the well, with no buried layer formed at an interface between the epitaxial layer and the substrate.

55. The trenched field effect transistor of claim 47, further comprising:

an epitaxial layer having the first conductivity type formed between the substrate and the well,

wherein the second depth relative to a depth of the well is adjusted to eliminate the need for any layers disposed between the epitaxial layer and the substrate.

PRESSE-SPIEGEL

PUBLIKATION / *PUBLICATION* : Electronics Weekly, UK

AUFLAGE / *CIRCULATION* : 31.721

AUSGABE & ERSCHEINUNGSDATUM : February 25, 1998

ISSUE & DATE OF PUBLICATION

Power FETs in Pentium push

Steve Bush

MOTHERBOARDS ARE becoming a target for application-specific power FETs. Both Siliconix and Fairchild have announced products aimed at Pentium-class processors.

Siliconix is claiming a record for on-resistance in DPAK packaging for its pair of MOSFETs for the CPU. The devices, built on Siliconix's 32m-cell trench technology, have an on-resistance of 7mΩ for the n-channel SUD50N03-07 and 10mΩ for the p-channel SUD45P03-10. Both of these maximum ratings are said to be the lowest in the industry for a power MOSFET in this package.

Fairchild's offering is the TO-220 packaged FDP7030. Still unvailable, it is part of its new PowerTrench range and slated to be a 30V MOSFET optimised for fast switching power converters on motherboards.

Siliconix's TrenchFETs can handle approximately a third more current than its previous-generation for the same dissipation and are aimed at powering CPU's in desktop computers.

"For generic motherboard manufacturers, these devices will spell the difference between a very complicated solution and a very simple one as they begin making motherboards with the next high-performance processor from Intel and other suppliers," said Phil Dunning, product marketing director at Siliconix. Samples and production quantities of the Siliconix FETs are available now, Fairchild's is due later this year.

See Technology p18

PRESSE-SPIEGEL

PUBLIKATION / *PUBLICATION* : Electronics Weekly, UK

AUFLAGE / *CIRCULATION* : 31.721

AUSGABE & ERSCHEINUNGSDATUM : February 25, 1998

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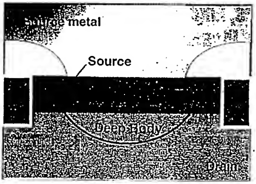
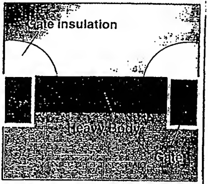


Structure Fairchild Semiconductor has produced its first commercial power MOSFETs using trench structures. Called PowerTrench, the range includes what is claimed to be the smallest ever 9mΩ power FET, the SSOT-8 FDR4420A. Low gate charge variants of some of the FETs are said to offer efficiency gains in DC/DC converter applications. A 3.5mΩ, TO-220 device is promised which should be the lowest resistance in this case size when it appears.



Trench warfare

With a shift from conventional cellular layout to a linear array design, Fairchild Semiconductor has put more gate lengths onto its trench power FETs cutting down their on-resistance. Steve Bush *reports*

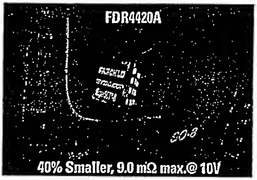
Yet another maker of power FETs has gone over from planar to trench structures for its low voltage devices.

This time it is Fairchild Semiconductor, formerly the discrete, memory and logic arm of National Semiconductor, for its new PowerTrench range of power FETs.

All other physical things being equal, trench structures have a lower on-resistance per unit area than planar structures because the current path through trench devices is shorter.

Fairchild has also gone away from the conventional cellular layout of features and adopted a linear array instead, with long straight gates stretching right across PowerTrench in parallel rows. SGS-Thomson has taken a similar approach with its planar power FETs. This kind of layout is variously called linear, strip or stripe.

Going to strip has allowed Fairchild to fit more gate length onto its chips. "There are several feet of gate on each chip," said Izak Bencuya, manager of the company's FET design centre.



More gate length means less on-resistance, the parameter that power FETs tend to be judged by. The reason that more gate length has been squeezed on, according to Bencuya, has a lot to do with going from cellular to linear structures, but the reason is not straight forward.

One of the problems with designing trench power FETs is breakdown voltage control.

All FETs will eventually breakdown as drain voltage rises. To ensure high device reliability, this breakdown must occur between source and drain. "With trench structures, the proximity of the bottom of the gate trench to the drain contact on the substrate encourages damaging gate-drain breakdown. The usual answer is to dope a deep 'body' between the gates to encourage source-drain breakdown to happen first," said Bencuya.

Fairchild says that conventional wisdom is that the deep body must be deeper that the gates. This indirectly sets the minimum gate-to-gate distance as the deep body diffuses in all directions equally during manufacture and cannot be allowed to reach the gates where it would ruin the device (see diagram). "A 3μm deep body has to be 6μm wide which [illegible] gate-to-gate distances [illegible] minimum of 6μm," said Bencuya.

Fairchild [illegible] PowerTrench has what it is calling a "heavy body", which is shallower than the gates. Bencuya said: "If the heavy body only needs to be 1μm deep, it is then only 2μm wide and the gates can be 4μm apart." Halving the gate-to-gate spacing means doubling gate length in a given area and halving the associated R_{DSon}.

Bencuya explained the reason that his body's can be shallower: "In a strip layout the body is a cylinder which can be arranged to breakdown in a more useful fashion that the spherical bodies that result in cellular FETs [illegible]

Trading R_{DSon} can gain efficiency

FAIRCHILD HAS [illegible] some of [illegible] PowerTrench FETs [illegible] gate charge [illegible]

The low gate [illegible] FET can show efficiency gains in high frequency switching power supply designs where gate charge current is significant compared with device I^2R losses.

The company is claiming an efficiency gain of over one per cent between one and 3.5A when its low capacitance FDS[illegible] FET is used [illegible]

This may not seem much, but the converters overall efficiency peaks at 93 per cent normally - a one per cent gain here is a 14 per cent reduction in losses.

Hitachi claims record breaking 4GHz superconducting ATM switch

Hitachi is claiming to have fabricated an experimental superconducting ATM (asynchronous transfer mode) switch that operates at 4GHz.

The previous record holder was another superconducting switch, operating at 3.5GHz. Non-superconducting compound semiconductor ATM switches stall at 2.5GHz.

The company points out that while optical fibres make the commercial transmission of data at 1Tbit/s foreseeable, conventional CMOS parallel switches will not be able to cope because of the increasing difficulties with packaging and heat. Superconducting devices can operate far faster than CMOS and with significantly lower power consumption.

The Hitachi device is said only to dissipate 1mW, despite operating at 4GHz and having 176 gates.

The switching elements are Josephson devices, which are superconductors split by a tunnelling insulator. The magnetic field of these can only exist as set quantum states and can therefore be used to store data.

The arbitration logic sorts input packets in order of address value, while crossbar switches direct them to their final destination. To avoid collisions, [illegible] packet pair attempting to leave for the same address is temporarily stored in a shift register.

The work is part of an MITI programme supported by the New Energy and Industrial Technology Development Organisation.

Fairchild Offers 9mΩ Power MOSFET

Fairchild Semiconductor Corp (www.fairchildsemi.com) of the US has been introducing progressively lower on-resistance power MOSFETs to the market. Following the FDS6680A with only 9.5mΩ on-resistance, the firm has introduced the FDR4420A, further minimizing on-resistance to 9.0mΩ or less. It also offers a superSOT-8 package which is 38% smaller than the standard SOT-8 package.

12% Annual Growth Market

From 1996 to 1999, the power transistor market is projected to grow 12.5% annually, and Fairchild Semiconductor is poised to gain a stronger position in three strategic markets: standard CMOS logic, discrete & EPROM/EEPROM, and analog & mixed signal.

The discrete market is very competitive. The top ten players dominate only 40% of the market. Fairchild intends to compete with a proprietary chip design and smaller package solutions.

For discrete power transistors, DC-DC converters and power supplies for mobile equipment are major applications. These markets require higher efficiency and a smaller footprint, which in turn, means longer battery life and higher packing density. Higher packing density is achieved with highly integrated semiconductor chips, and longer battery life is achieved with lower loss in the power source. Notebook computers, for example, have reduced power supply voltage with higher current capacity, following the same trend as Intel Corp (www.intel.com) of the US's Pentium microprocessors. In other word, lower loss is crucial.

Supporting PWM

This means DC-DC converters and power supplies should handle larger current and lower voltage. For power transistors to drive DC-DC converters and power supplies, lower on-resistance and higher switching speed are required to lengthen battery life, and to support pulse width modulation (PWM) switching at higher frequency.

PWM support is also key for notebook computers. Recent notebook computers with Pentium II microprocessors generate multiple supply voltages such as 1.8V, 2.5V and 3.3V. Changing duty ratio of PWM pulses generates multiple voltages.

Fairchild power MOSFETs feature lower on-resistance and gate charge to support higher speed operation.

Under a 10V gate voltage, The FDR4420A features the lowest on-resistance, 9mΩ and 41nC gate capacitance, and the FDS6680A offers lowest gate capacitance, gate capacitance 37nC and 9.5mΩ on-resistance.

A PWM DC-DC converter application requires two types of power transistors; high-speed switching and low conduction loss, and lowest conduction loss. FDR6680A is suitable for the former transistor application, and FDR4420A for the latter application.

The superSOT-8 package of the FDR4420A measuring 4mm x 3mm is unique, but the firm has applied to the Joint Electron Device Engineering Council (JEDEC) for a ruling on standardization.

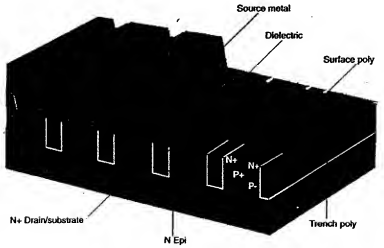
Similar to DRAM

A power MOSFET is equivalent to parallel connected small signal transistors, similar to DRAM memory cells, says Izak Bencuya, director of MOSFET Business Unit at Fairchild Semiconductor. The larger the number of transistors, the larger the current capability. The key issue is maximizing the current capacity over a limited chip area while minimizing the price.

Fairchild developed a trench structure along with layout improvements to boost the number of transistors in a given area.

The trench transistor (see Fig) sends current in a vertical direction, not in a planar direction. In conventional planar double-diffused MOS (DMOS) transistors, current flowed to both vertical and horizontal directions. The Fairchild trench transistor operates in a vertical direction mode. This method requires no space for horizontal direction current flow, and results in a reduction of the planar area in a transistor cell.

To reduce on-resistance and gate capacitance, the firm uses a shallow trench. The layout structure also enables high packing density of cell transistors.



Fairchild Power Trench Transistor

by Kenji Tsuda

PRESSE-SPIEGEL

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Flexible resistance in trench technology

by Nick Flaherty

Getting the lowest on-resistance for a power MOSFET is not necessarily the best parameter for power designers, according to Fairchild Semiconductors, as it launches its power manufacturing process.

Nearly a year on from its split from National Semiconductor, Fairchild Semiconductors has developed its own trench technology that is optimised for either low on-resistance or a combination of low on-resistance and low gate charge.

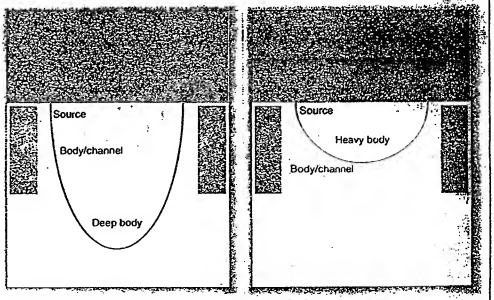
This second parameter is key for switching applications such as DC/DC converters, particularly as designers move up from 300kHz to 1MHz designs.

Fairchild has worked closely with Maxim on pulse width modulation controllers and found that some MOSFETs with an on-resistance of 22mΩ produce a more efficient switch than those at 12mΩ, due to the higher capacitance on the gate.

One of the first devices from the optimised PowerTrench process has an on-resistance of 10.5mΩ but a gate charge of 36nC, figures achieved by changing the thickness of the gate oxide.

This compares to a 55nC gate charge for the equivalent 8mΩ part in the standard process, and gives at least a couple of percentage points increase in overall efficiency.

Fairchild has combined the two parts on a single lead frame in a single package for such DC/DC converter designs. That is not to say that Fairchild is not also playing the minimum on-resistance game as well with the new process, as it plans to have a 3.5mΩ part for automotive applications, delivered in a TO-220 package.



The conventional trench at left is what we know. The flat bottomed trench is the new process from Fairchild. The fact that the trench appears to cover the source in these diagrams is a result of trying to represent a 3D process on a 2D chart.

The trench process uses stripes rather than a cellular structure and so Fairchild is defining the on-resistance of the process as 0.5mΩ/mm sq rather than in a cell density.

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Feature: POWER SEMICONDUCTORS

PowerTrench mosfets deliver lowest on-resistance plus fast switching

Fairchild has developed two new mosfet trench processes that deliver a very low on-resistance, while maintaining very fast switching performance beyond 1MHz. Called PowerTrench and Pwm PowerTrench, the processes use a non-cellular trench structure, rather than the cell-based trench processes used by competitors, to deliver a range of very small, high performance, high efficiency mosfets for the portable market . Chris Evans-Pughe reports.

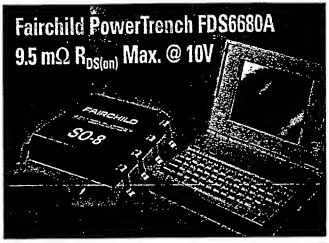
Initially targeted at 30 and 40V applications, typically, portable computing, dc/dc converter modules and high performance processor power supplies, Fairchild's latest mosfet technology has been under development for a year. PowerTrench is for high current applications and lower frequency switching applications, while Pwm PowerTrench, which features an ultra low gate charge, with a slight reduction in on-resistance, is optimised for high efficiency, high frequency power switching applications.

"Although we are focussing on 30 and 40V initially, it will be quite easy to convert the technology 60V if necessary. Trench processes only make sense up to 100V, but that covers a very large part of the market", commented Frank Marx, Fairchild's director of marketing for discrete power and signal technologies.

The first products built on the new processes are sampling now, with volume available very shortly. They include the 30V, FDR4420A, which comes in Fairchild's tiny SuperSOT-8 package, which is 38 percent smaller than an SO-8. The n-channel device is claimed to be the smallest ever 9mΩ mosfet. The 9mΩ maximum on-resistance is achieved at 10V V_{GS}, and it rises to 13mΩ at 4.5V V_{GS}. The gate charge is 42nC. The device is particularly well suited to low voltage and battery powered applications where small package size is required without compromising power handling, in-line power loss or fast switching.

Another new device is the FDS6670A, which at 8mΩ maximum $R_{DS(ON)}$ (V_{GS}=10V) is claimed to offer the lowest on-resistance in SO-8. Finally, there will be the 30V, FDC6655N available in the miniature SuperSOT-6, which is 72 percent smaller than the SO-8. This mosfet features an on-resistance of 25mΩ at 10V V_{GS}, and 33mΩ at 4.5V V_{GS}.

In the Pwm optimised PowerTrench range, Fairchild is introducing the SO-8 packaged FDS6680 which provides the dc/dc designer with low on losses and low switching losses. Features include an on-resistance of 9.5mΩ at V_{GS} = 10V, combined with a very low gate charge (41nC, typical), fast switching speed, and high power and current handling capability. Other specifications include TDelay On = 8ns, TRise =32ns, TDelay Off = 42ns and Tfall =14ns. By using this device, designers will achieve a significant improvement in efficiency, resulting in longer lasting batteries and cooler running systems, according to Fairchild.



As an example of how the FDS6680A compares to competitive parts on the market, Temic's Si4420 trench mosfet features a 9mΩ on-resistance with a 70ns gate charge, while the company's Si4410 has a 13.5mΩ on-resistance with a 35ns gate charge.

Designers can increase efficiency simply by changing the mosfet in their design to a device in Fairchild's PowerTrench family, says the company. Other parts are planned for addition to the PowerTrench family in the near future.

Fairchild
Write in number 450

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What's Hot

高科技產業求才若渴

近年，國內華碩電腦、台積電等公司員工分發股票、紅利之狀況令人稱羨，引發高科技及周邊人才競相投入。此舉乃繼前幾年金融服務業年終分紅十數月薪，有過之而無不及。現今就業市場掀新洗牌之效應傾向，資訊電子產業、金融服務業取代傳統製造業而專美於前，人才精英再創高附加價值，維持勞資雙方良性互動，才是壯盛產業經濟之道。P21

100MHz P II晶片組問世

由於英特爾 Pentium II 級 BX 晶片組將在年中問世，晶片組廠商無不急思對策，以因應即將來臨的戰火。繼先前推出 100MHz 的 Socket 7級晶片組Aladdin V(阿拉丁五代)之後，國內的揚智科技(ALi)更在日前推出一款該公司第六代的產品Aladdin Pro II，以Slot 1級BX相容晶片為號召，為倒數計時的戰事提前準備。其所搭配的M1543C南橋晶片更延續了以往阿拉丁系列的特點，將SuperI/O整合到晶片組之中，係為此一晶片組的特色。 P8

國產相片印表機出爐

台灣產業在影像輸出裝置之一的印表機上一直處於落後的地位，較之日商根本毫無出手的機會。不過此情形即將改觀，包括鴻友科技、台灣半導體、華成光電將在今年下半年相繼推出相片印表機，以乾式相紙為列印材質，全國打進一般消費性產品市場，讓影像輸出品質更佳、更容易保存，同時緊密結合影像的輸出及輸入功能。廠商正摩拳擦掌地計畫於下半年正式量產 300dpi 熱感式相片印表機。 P6

號外

台北國際電子展
展覽期間 3/20-3/24
推出「電子展特輯」
現場以七折特惠價
回饋讀者

Software modem/RISC combo is cost-efficient
Strong ARM excels with 12-bit Booth's multiplier

Processor	MAC resolution	Cycles	Actual time (μs)	Early terminate?	Processor speed (MHz)
ARM/Digital StrongARM	32x32 64-bit·64-bit result	2 to 5	10 to 25	Yes	233
NEC VR31100 (Mips)	32·32or16·16· 64-bit result	1 (assumed)	25	Unknown	40
Hitachi SH-3	32x32 64-bit+64-bit result	2 to 5	44 to 67	Yes	45
Motorola MPC821	16·162-40-bit· 40-bit result	1	20	No	50

▲軟體數據機 /RISC 組合具成本效益　　P47

數位相機OEM 商機登台

據傳美、日大廠有意將低階機種委託台商製造

【本刊編輯高瑤芬報導】外傳美商數位相機大廠 Kodak 基於成本的考量，有意委託台灣方面生產中低階產品，高階產品則仍繼續留在本國生產。對於此一傳聞，國內供應商諸多保留，不願正面回答。然而同時卻又傳出日商也有意來台採購，而源興極有可能因此出線，在四月間獲致重大進展。

如同掃描器的情況一般，在低階產品價格滑落，利潤有限的情況下，而台灣廠商技術能力也有一定水平後，日商便紛紛來台尋找代工夥伴，台灣因此一躍而成掃描器全球主要供應商之一。

而今年日本數位相機主要供應商將陸續轉戰高利潤百萬像素機種，對於低階入門機種則[illegible]委外生產，藉以降低生產成本，以反應日益滑落的售價，其中又以台灣最受日商青睞。

據聞，Kodak 目前曾與鴻友科技針對此事加以協商，不過因為日方報價遠低於廠商期望，而鴻友又因憑藉著掃描器建立起來的知名度，心想主打自由品牌，不斷在價格上多所退讓而作罷。此外，國內另一數位相機供應商普誼光電則不斷 文轉第10頁

嘉畜廠閒置 同業鳴不平

台積電原可望二月底敲定買主，翁家內部卻傳出異議

【本刊訊】在新竹科學園區一地難求之際，嘉畜預定興建的八吋晶圓廠廠房及土地卻閒置不用，受到各方批評。為了順利解決這個問題，一年前由園區管理局出面，撮合聯電和台積電購買嘉畜廠房，不過目前得知聯電早在去年退出競標行列，而台積電和嘉畜原有意在二月底決定買賣，但因為嘉畜眾翁家家族人員共識不一，使得此案子可能胎死腹中。

> 台積電高層主管表示，目前雙方合作與否已經不再適合由台積電發言，應該由翁小姐來主導。

聯電董事長曹興誠曾在去年聯電記者會上回答記者有關購併嘉畜廠事宜時表示，由於嘉畜和聯電雙方在買賣嘉畜晶圓廠的事件中難以達到共識，所以聯電集團放棄與嘉畜繼續進行談判事宜，並不再考慮購買這座廠房，而使得這項合作計劃中止。

不過台積電卻一直對這座晶圓廠的購併案有著高度的興趣，所以在聯電正式退下談判桌後，台積電高層仍不斷與嘉畜高層進行深度的意願和條件溝通。

這件案子不論是園區管理局、台積電或嘉畜內部都是樂觀其成的合作案，但是就在華隆微集團也是嘉畜總經理翁大銘原則同意雙方合作條件之際，翁家二小姐突然加入談判行列，使得這個原本已經打算在近期內順利完成的合作案，可能告吹。

台積電高層主管表示，目前雙方合作與否已經不再適合由台積電發言，應該由翁小姐來主導。事實上由於這件案子充滿了各種變數，所以台積電將積極轉往台南興建晶圓廠，以應付未來市場成長的需求。 文轉第11頁

快捷新推MOSFET 搶攻NB零件市場

【本刊記者翁蕙茹報導】歷經多次被併購及轉售命運之後，快捷(Fairchild)終於重出業界，打算在今年利用最新的 Power-Trench 技術，搶攻筆記型電腦、PDA、HPC 及交換式應用等市場，必須採用的 60V 以下低電壓 MOSFET，取得同業領先的地位。

Fairchild 離散功率訊號技術市場協理 Frank Marx 表示，縱使 IR、Temic(意指 Siliconix)及 Motorola 等前十大 MOSFET 供應商在業界享有一定的知名度，但所佔的市場佔有率也不過百分之四十，所以對 Fairchild 而言，擁有非常好的切入機會點。

根據 Dataquest 統計的全球小訊號元件和離散式功率元件市場顯示，未來二年功率元件的複合成長率將達到百分之十二點五，而小訊號的複合成長率則為百分之九點三。雖然成長的幅度不算大，但由於現有廠商的投資意願不高，所使用的技術也較傳統，所以面對所有新的設計迴路，有時候難以因應。

Frank 進一步表示，Fairchild 結合新一代的 PowerTrench 的技術，適時的解決現階段 Intel、AMD、Cyrix 及 IDT 等 CPU 技術發展瓶頸。事實上，由於半導體製程不斷的朝高集積度發展，使得利用 CMOS 製程的 CPU 無法承受過 文轉第10頁

標準底定 頻道支援

視訊解碼器內銷需求浮現

【本刊訊】視訊解碼器(set-top box,STB)在國外行之有年，自發展開始至今，類比式STB銷售量已累積至1200萬台，尤其集中於英國及德國地區；不過台灣生產STB多年，卻始終無法打開國內市場。然而前有一月份數位電視發射系統標準底定，加上後有頻道業者如：力霸與TVBS有意支援等雙重誘因刺激下，因此國內STB出貨量可望大為激增。

STB主要可分為兩種，一用於接收衛星傳送的訊號並加以解碼，另一種則是接收利用有線傳送而來的訊號並解碼，經由電視輸出影像。而兩類又各有數位與類比的差別。

以數位STB而言，目前歐洲及北美地區因為發射的衛星多，可接收的節目也多，因此搭配著頻道業者裝機 文轉第10頁

聯電慷慨放送 聯瑞股東獲利

為彌補火災股東損失， 將以關係企業股票轉換為保證

【本刊記者翁蕙茹報導】為安撫聯瑞策略聯盟的建廠大股東免於疑慮，聯電集團在聯瑞失火後，主動提供策略聯盟的股東二種選擇條件，一為免費升級原有合約製程由0.35微米至0.25微米和0.18微米，二為如果三年後聯瑞獲利不彰，則由聯電集團提供本身的聯誠股票，以一股換一股的方式將股東手中聯瑞的股票換成聯誠股票。

事實上，由於今年美國半導體產業的表現不甚理想，尤其繪圖晶片業者因為產品改朝換代，出現了洗牌效應，造成原本在市場主流的廠商受到極大的衝擊。由於如此，據傳聯瑞原有的 Fabless 大股東對於聯瑞的增資案興趣缺缺，連同去年在繪圖晶片市場表現最好的 ATI 也不願意再繼續加碼投資。

聯電集團雖然傾全力提供聯瑞客戶可供生產的晶圓廠，但由於目前聯電集團較穩定的製程技術在聯誠，其他聯嘉和合泰都在最近才試產成功，因此多數客戶並不願意轉移已經在市場上成熟的產品至新的晶圓廠生產，加上目前市場上晶圓代工產能易覓，Fabless 設計公司選擇多，除非價格極具吸引力，否則不會挑選新晶圓廠下單。

經由向多家與聯瑞策略聯盟的大股東私下求證，得知目前大家對於聯電集團所提供的免費升級至下一代製程的條件接受意願並不高，多數打算採用乙案以聯瑞股票一股換一股方式直接獲利了結。

聯電集團高階主管表示，為了使聯瑞股東能夠安心，所以聯電集團主動提出二項條件讓股東有所選擇，而事實上，三年後如果股東打算換股，也是聯電集團由本身所擁有的股份移轉，整個事件僅為個案，並不會直接影響投資大眾的權益。

服務至上 天騰提供全方位方案

▲ Compaq 技術服務協理楊林森

【本刊編輯柳林緯專訪】日前傳出Compaq與迪吉多創下天價的九十六億美元合併案，已引起多方的關注，各界均不斷揣測可能的後續結果。由於Compaq在去年併購以企業用戶爲主的Tandem，一般預期這將會是日後迪吉多可能的處理模式。以下就是本刊對此採訪負責Tandem相關產品的Compaq技術服務協理楊林森之摘要。

問：依您來看，這次Compaq與迪吉多的合併案是否樂觀？

由於迪吉多已經與我們合作多年，而且該公司本身就是MCS（Multivender Customer Support）的角色，這樣的合併，對於以往偏向銷售的我們來說，應該是非常看好的事。此外，對於我們在公元兩千年將要達到的五百億的水準，如果只偏重銷售而忽略客戶服務，我想大客戶是不會滿意的，所以，這對我們來說是非常樂觀的合併案。

問：就目前而言，天騰（Tandem）與Comapq合併至今情況如何？

我覺得彼此地相處得融洽的，公司間的文化差異雖然還需要一段時間才能完全的融合，但我想這是沒有任何問題的。如同日後與迪吉多的合併案成立後，這樣的模式就可以複製到迪吉多上面了。至於在產品方面，天騰與Compaq的Windows NT產品整合成功，就提供客戶全方位的解決方案來說，成果及前景都是非常豐碩的。

問：您剛剛提到的全方位解決方案，天騰目前有何計劃或動向呢？

最近我們在推的解決方案有三個，分別是：電子商務（EC：Electric Commerce）、電話服務中心（Call Center），以及公元兩千年（Y2K）解決方案。電子商務的需求已受到重視；而在電話服務中心方面，近來蓬勃發展的信用卡、民營電信、大眾服務業，就非常適合；至於公元兩千年的問題，我覺得是最受到忽略的，所有廠商都應該正視這個問題，否則到時候就來不及了。

Rambus路迂迴 Intel改其道而行

【本刊譯】將800MHz Direct Rambus記憶體技術帶進個人電腦主流市場的路途在Intel Developers Forum上應該會更顯崎嶇。英特爾宣佈將發表一項計畫，將同步DRAM裝置在100或133 MHz Rambus模組上，讓SDRAM實際上模擬Rambus架構。在此同時，英特爾也正在考慮將66MHz SDRAM規格加入其即將發表的440BX晶片組中。此型晶片組原本僅適100MHz SDRAM。

由於SDRAM價格急速下降，使得裸晶尺寸較大、封裝與測試費用較高、權利金支出也較多的Direct RDRAM越來越不可能很快地進入主流桌上型電腦市場，這使得英特爾不得不採取一些應變的措施。另外，一千美元以下的個人電腦正日漸受到歡迎，英特爾更必須與更低成本記憶體與晶片組來勢洶洶的對手競爭。

英特爾原本計畫在1998年年初將個人電腦業界由66MHz轉移到100MHz SDRAM，接下來在1999年再很快地轉換爲800MHz Direct RDRAM。但即使連英特爾本身的工程師都意識到Rambus計畫可能會發生一些延遲。原先促使該公司支援Rambus方案的因素，包括接腳數較少以及頻寬更高等，目前看來仍然佔有相當大的優勢。

某些消息來源在國際固態電路研討會中指出，混合式SDRAM/Rambus中程解決方案即是利用目前最快的SDRAM，裝置在Rambus排裝記憶體模組(RIMM)之上。英特爾還會在RIMM上加入一個轉換IC，將SDRAM的資料輸出轉換到控制邏輯電路上的Rambus ASIC單體(或稱RAC)。SDRAM一般只有六十四位元資料匯流排，而Rambus則使用十六位元匯流排。如果使用錯誤檢查控制(ECC)時，則匯流排爲十八位元。

批評此種方案的人士表示，額外的邏輯會增加成本，同時也會在記憶體與處理器之間造成多達10ns的延遲。

在此同時，英特爾也宣佈將此方案加入其下一世代記憶體控制器（440 BX）中，讓個人電腦OEM廠商使用不同速度等級的SDRAM以及Direct RDRAM。英特爾原本計畫僅支援自己版本的100MHz SDRAM規格（稱爲PC/100），供專爲100MHz設計，即將推出的BX晶片組使用。但現在該公司正考慮加入讓記憶體匯流排能夠在Jedec所制訂的66MHz SDRAM上執行。

英特爾目前顯然有相當強烈的意圖要將66MHz規格包含在內。DRAM製造業界的消息來源指出，這家微處理器的領導廠商僅授權數家DRAM公司使用其PC/100規格，並且將發供應短缺可能會導致DRAM價格大幅上漲。英特爾以前已經進行許多工作，但是再有任何延遲的話，就可能造成來自OEM廠商希望將系統升級爲100MHz匯流排的反彈。

CMP Article

快捷新推MOSFET

▲ Fairchild離散功率訊號技術市場協理Frank Marx

文接第1頁　的電壓值，則由於CPU設計的複雜度及閘級數(Gate Count)不斷增加，造成流入的電流值必須加大，使得CPU和Core Logic產生發熱的現象，影響了系統的穩定度，這時透過一顆可耐高功率的MOSFET IC，便成了穩定系統不可缺乏的關鍵因素。

Frank指出，以往由於製程技術的限制，使得MOSFET利用SO-8的設計只能維持在一千萬電路細胞元件(Cell)而難以突破，但一旦使用了PowerTrench的新製程技術，則可以提供至三億二千萬電路細胞元件。

經過這樣的製程技術革新，Fairchild能夠提供客戶高品質且具市場競爭力的產品，同時在縮小元件面積和包裝、整合度、熱阻抗及散熱等特性上，均可提供更有彈性的電路設計組合。

Frank進一步強調，Fairchild透過PowerTrench的技術，將爲客戶帶來改善元件執行效率、增加系統散熱性及延長電池使用壽命等優點。

雖然目前在市場難免有一些競爭對手，但Frank認爲，由於Fairchild不採用競爭對手的蜂狀結構，而改採條狀結構式設計，使得散熱問題處理變得簡單、而且面積變小、成本降低、導電損耗低及切換損耗減小，再經過製程的PN接面(Junction)面積縮小，可使得元件漏電電流大幅改善。

封面新聞

嘉畜廠閒置 同業鳴不平

文接第1頁　曾參與這項談判過程的嘉畜代表私下也表示，自從Sony與嘉畜品牌廠策略聯盟之後，不論華隆微或嘉畜員工，皆樂於見到已完成廠房外形的嘉畜晶圓廠，能夠早日順利裝機，加入量產行列，以擺脫過去在園區被視爲不良的印象。不過，二小姐加入後，使得這項計劃變得流於形式、繁複，並讓整件合作案陷入膠著。

據了解原本嘉畜原則上同意完全轉讓現有土地及廠房給台積，但由於翁小姐執意嘉畜仍然要留在園區內，並維持一定比例的股權金額，故造成彼此共識難以達成。

至於雙方是否仍會成功達成合作共識，業界普遍的看法認爲要維持現階段的狀況，可能性不大，但如果翁小姐退出談判而轉由幕僚主導，才有轉圜的餘地。

標準大勢底定頻道支援

文接第1頁　的促銷，STB很容易深入到家庭；而大陸地區除了中央的電視頻道外，各省又有自己的頻道，也是廠商積極開發的重點市場。

可是唯獨台灣地區雖然包括亞視科技、大同、誠洲、宏碁、億華及泰山電子等，都相繼推出STB，不過市場卻都是以國外頻道業者爲主，以亞視科技爲例，目前才剛與南非電視系統業者Multichoice簽訂20萬台的數位STB的訂單，金額高達6千萬美金；另外誠洲每月出貨STB約5000台，市場則絕大多數在大陸地區。

STB的出貨對象並非一般家庭用戶，而是當地頻道提供者，若客戶提出收視申請，業者即派人前往裝設STB，之後便能收看節目。亞視科技副總陳信義指出，頻道供應商爲了擴展收視戶，並開發新客源，STB的價格自然不可能訂的太高，加上製造商本身材料成本的降低，STB將會朝低價發展。目前一個數位STB售價約在300美金上下。

因爲數位電視發射系統標準的底定，相信今年底將會有一些頻道業者發射數位訊號，另外九霸集團有意支援STB，加上旗下頻道提供者眾多，兩相配合之下，STB在台灣可望正式起步。

數位相機OEM商機登台

文接第1頁　對此事做正面回答。不過根據了解，力捷早於去年就接獲Mitsubishi小量數位相機訂單。

而新興廠商源興目前正與Intel合作一款既可當一般數位相機使用，又可以應用於視訊會議用途的多功數位相機，彼此間關係因此十分密切。根據相關人員表示，源興一向的策略是以承接OEM訂單爲主，數位相機的銷售策略也會是如此，而經由Intel從中牽線，源興可望於四月份正式簽訂數位相機訂單，至於細節問題，源興不願意透露。

根據業界人士表示，日商轉戰高階市場，將中低階產品委外生產是必然的趨勢，不過進入數位相機領域，必須同時具備光學、工業設計等技術能力，門檻並不低；而台灣整體數位相機產業在零組件的供應，甚至於基礎建設都還需更加健全才是，等到能力技術獲得提昇，相信以廠商的製造能力，未來成爲數位相機的主要供應國將是指日可待。

FPGAs融入標準IC變動

【本刊譯】由於複雜的核心在可程式化設計中所扮演角色越來越重要，晶片製造業的巨人Motorola及Lucent Technologies已經準備好要擴展現有在FPGAs方面選擇的範圍。

Motorola的半導體產品部門推出一款晶片上附有FPGA的ColdFire CPU。這項組合開創一條新的產品線，並在可程式邏輯趨勢方面帶領潮流。將來可能使得許多高階可程式邏輯方面的生意跑到標準產品IC業者手上。

據報導，Motorola結合了ColdFire的核心跟由他們的Pilkington延伸出來的SRAM-programmable FPGA邏輯陣列，這種結合一個32位元CPU跟FPGA核心到同一晶片中，可讓內嵌式計算系統客戶在微處理機的晶片上就可以完成自訂的匯流排介面、周邊模組及相關的功能，節省了多晶片核心系統所要必須花費的空間、速度及電力消耗。

FPGA區塊可能扮演的角色，將會是在從廣泛使用的68300家族到ColdFire產品線中加入的周邊模組。目前已經進行將68300周邊部分換成可合成的形式。

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